Field Effect Transistors

Lesson #9
MOSFETS
Sections 5.1-3

Homework

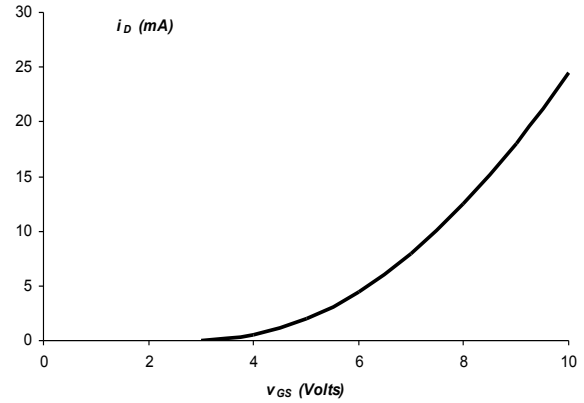
- NMOS Transistors
  - Problems: 5.3, 5.4, 5.6
- Load-line Analysis
  - Problems: 5.14-19
- Bias Circuits
  - Problems: 5.21, 5.23
- JFETs
  - Problems: 5.56, 5.57, 5.65
- CMOS
  - Problems: 6.48-6.50 6.69-6.70, 6.71-73

Homework Answers #1

- NMOS Transistors
  - Problems: 5.3 V_{to}=*1 V; KP=30mA/V*^{2}*, L=5mm, W=50mm*
    - Recall:
      - Cutoff: $v_{GS}=0$; $i_D=0$
      - Triode: $v_{GS} \geq V_{to}$; $v_{DS} < v_{GS} - V_{to}$;$i_D=K[2(v_{GS}- V_{to}) v_{DS}- v_{DS}^2]$
      - Saturation:$v_{GS} \geq V_{to}$; $v_{DS} \geq v_{GS} - V_{to}$;$i_D=K(v_{GS}- V_{to})^2$
    - $v_{GS}=4V$, $v_{DS}=10V$
      - $v_{GS}- V_{to}=4-1=3<10= v_{DS}$ *SATURATION*
      - $=(50/5)(30/2)(3^2)=1.350mA$
    - $v_{GS}=4V$, $v_{DS}=2V$
      - $v_{GS}- V_{to}=4-1=3>2= v_{DS}$ *TRIODE*
      - $i_D=K[2(v_{GS}- V_{to}) v_{DS}- v_{DS}^2] =(50/5)(30/2)[2(3)2-2^2]=1.20mA$
    - $v_{GS}=0V$, $v_{DS}=10V$
      - $v_{GS}- V_{to}=-1$ *CUTOFF*
      - $i_D=0$

Homework Answers #2

- NMOS Transistors
  - Problems: 5.4 $V_{to}=3\ V;\ K=.5mA/V^2,\ v_{GS}=5V$
    - Saturation: $v_{GS} \geq V_{to};\ v_{DS} \geq v_{GS} - V_{to}\ ; i_D=K(v_{GS}- V_{to})^2$
      - NMOS will be in Saturation for $v_{DS} \geq v_{GS} - V_{to}=5-3=2V$
    - Triode: $v_{GS} \geq V_{to};\ v_{DS} < v_{GS} - V_{to}\ ; i_D=K[2(v_{GS}- V_{to})\ v_{DS}- v_{DS}^2]$
      - NMOS will be in Triode Region for $0<v_{DS}<v_{GS} - V_{to}=5-3=2V$
    - $i_D=K(v_{GS}- V_{to})^2=.5\ (v_{GS}- 3)^2$

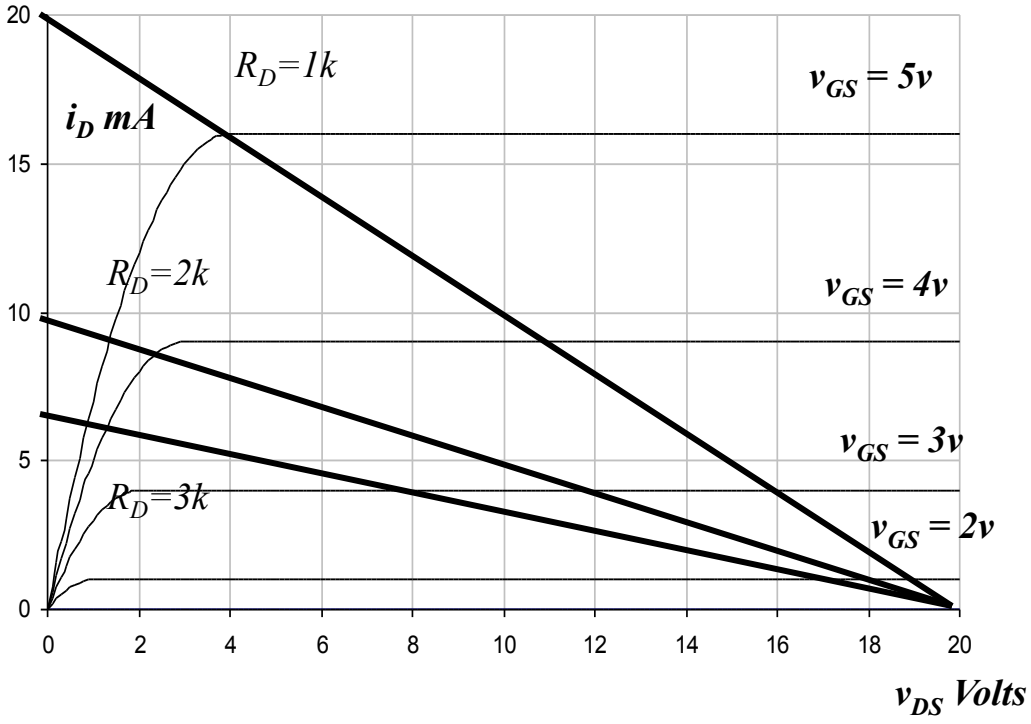


Homework Answers #3

- NMOS Transistors
  - Problems:5.6 $V_{to}=1\ V$
    - $v_{GS}=0V,\ v_{DS}=5V$
      - $v_{GS}-V_{to}=-1$ *CUTOFF*
    - $v_{GS}=3V,\ v_{DS}=1V$
      - $v_{GS}-V_{to}=3-1=2>1=v_{DS}$ *TRIODE*
    - $v_{GS}=3V,\ v_{DS}=6V$
      - $v_{GS}-V_{to}=3-1=2<6=v_{DS}$ *SATURATION*
    - $v_{GS}=5V,\ v_{DS}=10V$
      - $v_{GS}-V_{to}=5-1=4<10=v_{DS}$ *SATURATION*
- Load-line Analysis
  - Problems: 5.14
    - Distortion is a result of the curvature and non-linear spacing of the characteristic curves

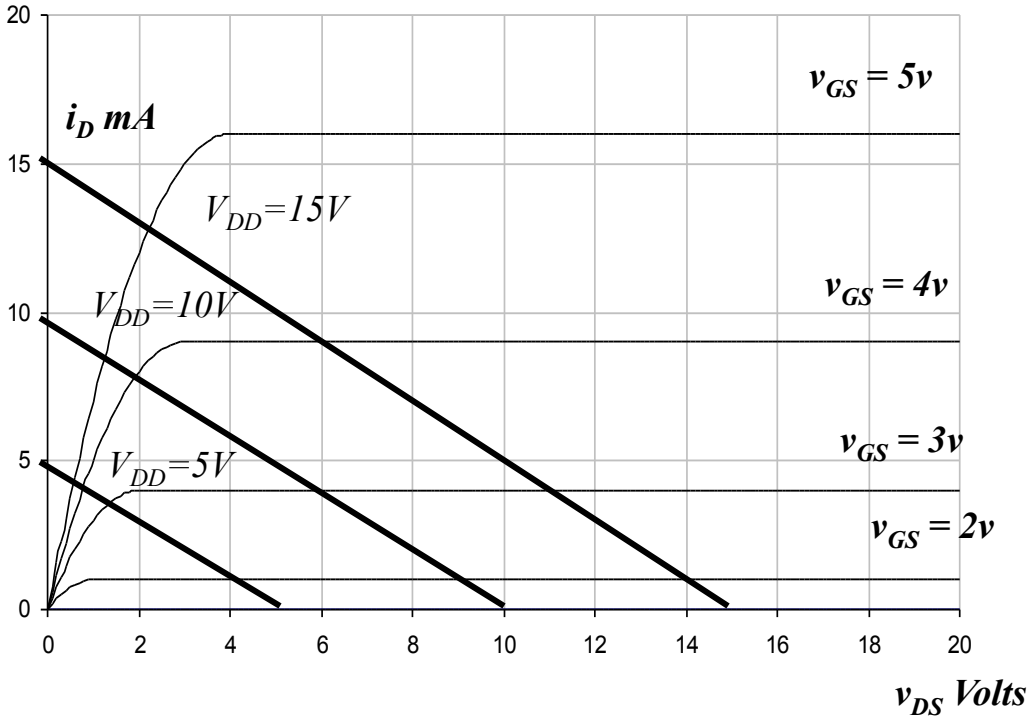
Homework Answers #4

- Load-line Analysis
  - Problems: 5.15
    - $R_D=1k$, $V_{DD}=20V$
    - $R_D=2k$, $V_{DD}=20V$
    - $R_D=3k$, $V_{DD}=20V$



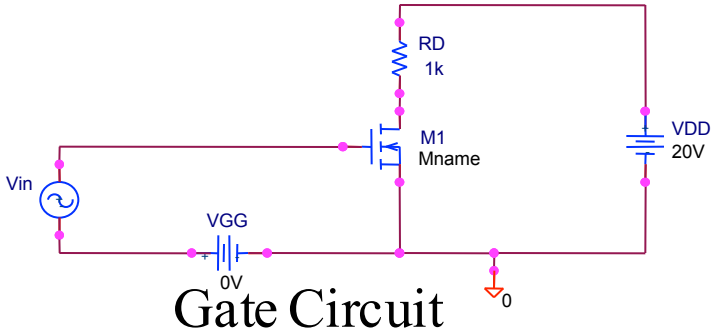
Homework Answers #5

- Load-line Analysis
  - Problems: 5.16
    - $R_D=1k$, $V_{DD}=5V$
    - $R_D=1k$, $V_{DD}=10V$
    - $R_D=1k$, $V_{DD}=15V$



Homework Answers #6

- Load-line Analysis
  - Problems: 5.17

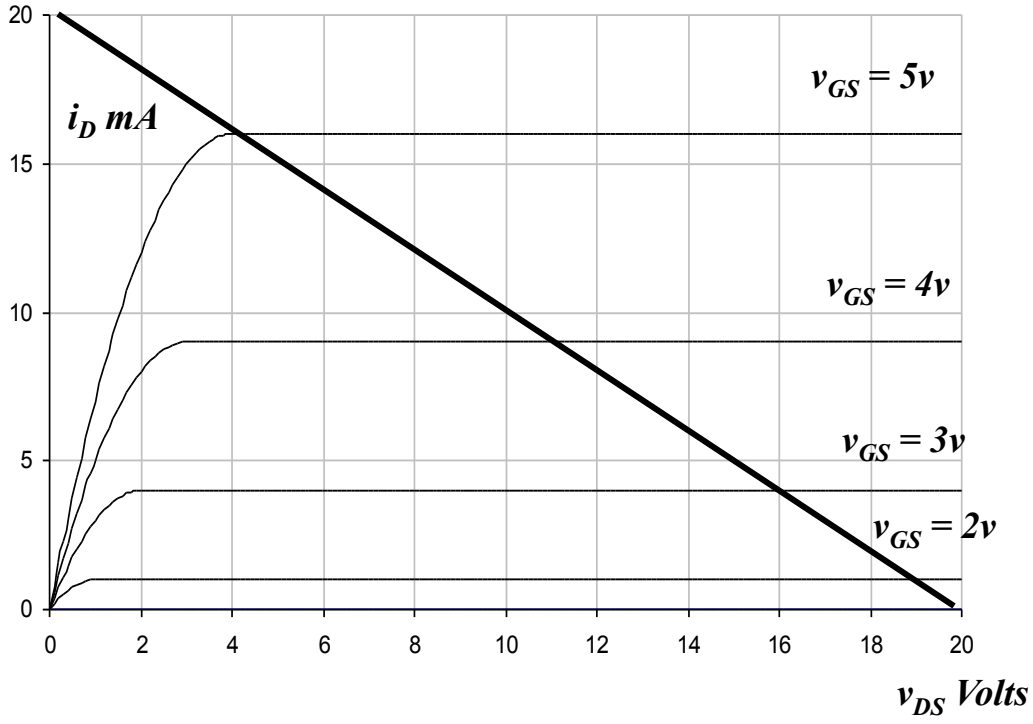


Gate Circuit

$$v_{GS} = v_{in}(t) + VGG$$
$$= \sin(2000\pi t)$$

Drain Circuit

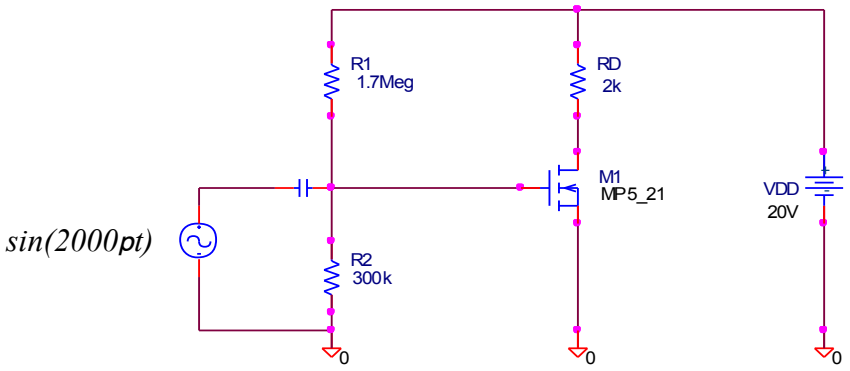
$$VDD = i_D RD + v_{DS}$$
$$20 = i_D 1000 + v_{DS}$$



Since $v_{GS} \leq 1 = V_{to}$, the FET remains in Cutoff. $V_{DD} = 20V$

Homework Answers #7

- Load-line Analysis
  - Problems: 5.18, $V_{to}=1\ V$, $K=.5mA/V^2$

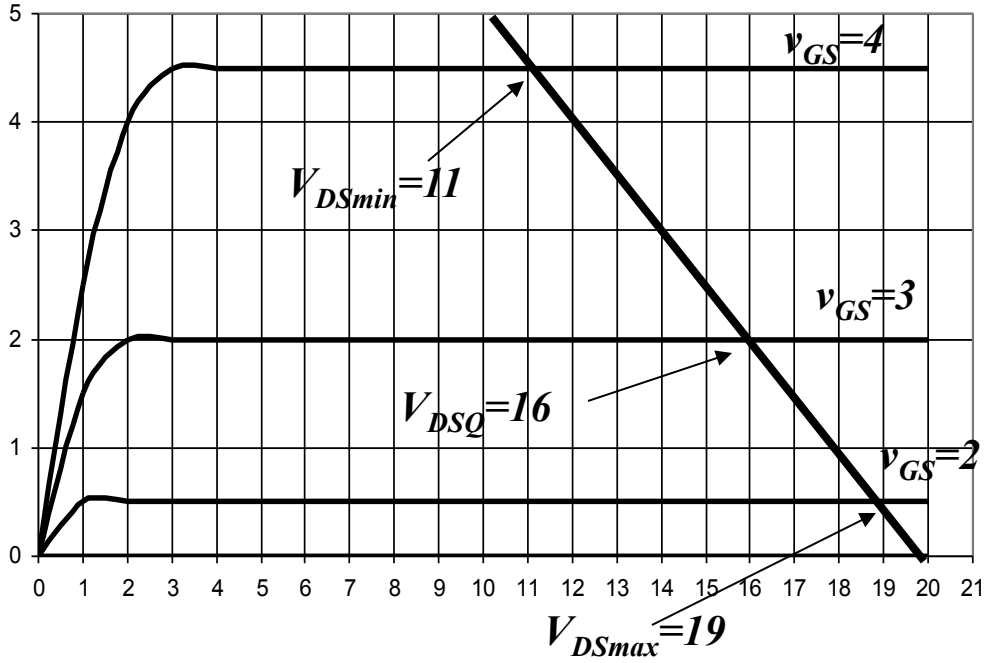


a) By Superposition

$v_{GS}(t)=3+sin(2000\pi t)$

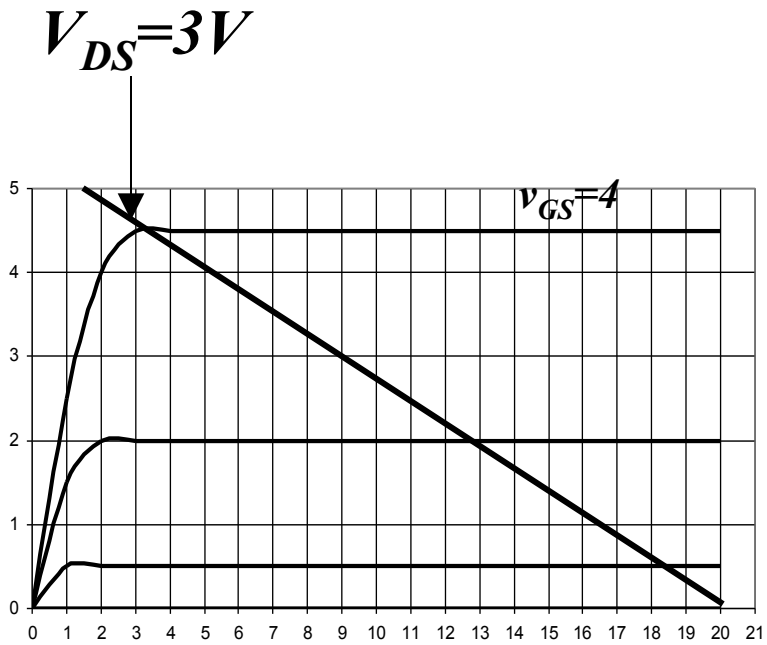
Homework Answers #8

- Load-line Analysis
  - Problems: 5.18 b-d)



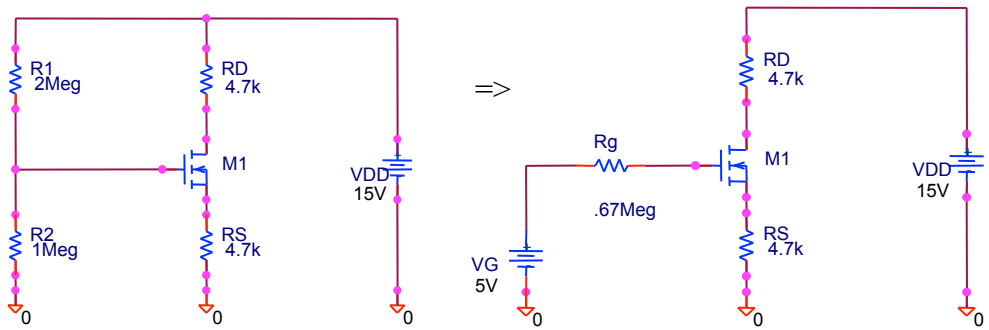
Homework Answers #9

- Load-line Analysis
  - Problems: 5.19, $V_{to}=1\ V$, $K=.5mA/V^2$
    - Move the load line to intersect V_{GSmax} at the edge of the Saturation region
    - Saturation: $v_{GS} \geq V_{to}$; $v_{DS} \geq v_{GS} - V_{to}$; $i_D=K(v_{GS} - V_{to})^2$
    - $V_{GS\,max} = 4 \geq V_{DS\,min} = 3$, $i_D=K(v_{GS} - V_{to})^2=.5(3)^2=4.5mA$
    - $RD\ max=(20-3)/4.5=3.778k\ \Omega$



Homework Answers #10

- Bias Circuits
  - Problems: 5.21
  - V_{to}=*1 V, K=.25mA/V²*



The voltage around the equivalent gate circuit :

$$VG = v_{GS} + R_S i_D$$

$$= v_{GS} + R_S K(v_{GS} - V_{to})^2$$

$$KR_S v_{GS}^{\ 2} + (1 - 2R_S K V_{to}) v_{GS} + R_S K V_{to}^{\ 2} - VG = 0$$

$$v_{GS}^{\ 2} + (\frac{1}{KR_S} - 2V_{to}) v_{GS} + V_{to}^{\ 2} - \frac{VG}{R_S K} = 0$$

$$v_{GS}^{\ 2} + (\frac{1}{2.35} - 2) v_{GS} + 1 - \frac{5}{2.35} = 0$$

$$v_{GS}^{\ 2} - (1.1489) v_{GS} - 3.2553 = 0$$

- Roots are v_{GS}=*2.468, -1.319*
- Choose v_{GS}= *2.468* since V_{GS}> V_{to}=*1*

$$I_{DQ} = K(v_{GS} - V_{to})^2 = .25(2.468 - 1)^2$$

$$= 0.5387 ma$$

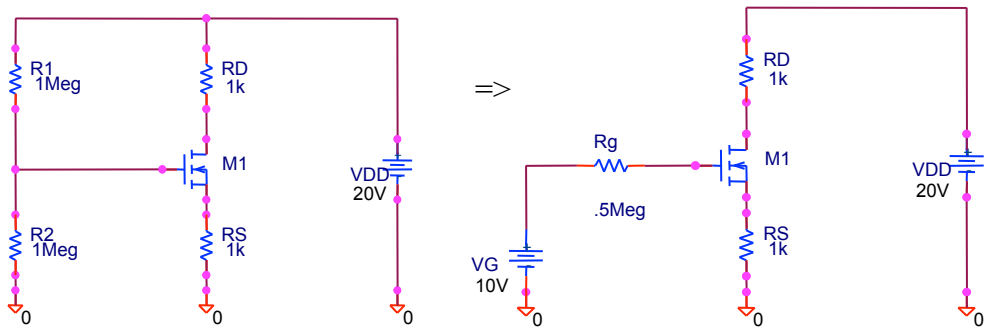
The voltage around the Drain Circuit :

$$VDD = V_{DSQ} + I_{DQ}(RD + RS)$$

$$V_{DSQ} = 15 - 0.5387(9.4) = 9.9359\, V$$

Homework Answers #11

- Bias Circuits
  - Problems: 5.23
  - V_{to}=4V, K=.25mA/V^2



$$VG = v_{GS} + R_S i_D$$
$$= v_{GS} + R_S K(v_{GS} - V_{to})^2$$
$$KR_S v_{GS}^{\ 2} + (1 - 2R_S K V_{to}) v_{GS} + R_S K V_{to}^{\ 2} - VG = 0$$
$$v_{GS}^{\ 2} + (\frac{1}{KR_S} - 2V_{to}) v_{GS} + V_{to}^{\ 2} - \frac{VG}{R_S K} = 0$$
$$v_{GS}^{\ 2} + (\frac{1}{1} - 8) v_{GS} + 4 - \frac{10}{1} = 0$$
$$v_{GS}^{\ 2} - 7 v_{GS} + 6 = 0$$

- Roots are v_{GS}=6, 1
- Choose v_{GS}= 6 since $V_{GS} > V_{to}$=4

$$I_{DQ} = K(v_{GS} - V_{to})^2 = 1(6-4)^2$$
$$= 4ma$$
$$VDD = V_{DSQ} + I_{DQ}(RD + RS)$$
$$V_{DSQ} = 20 - 4(2) = 12\,V$$

Homework Answers #1

- JFETs
  - Problems: 5.56, V_{to}=-3 V, I_{DSS}=9mA
    - Saturation: $v_{GS} \geq V_{to}$ and $v_{DS} \geq v_{GS} - V_{to}$, $i_D = K(v_{GS} - V_{to})^2$

$$K = \frac{I_{DSS}}{V_{to}^{\,2}} = \frac{9\times10^{-3}}{(-3)^2} = 1mA/V^2$$

$$i_D = K(v_{GS} - V_{to})^2$$

$$4mA = 1mA/V^2((v_{GS} - [-3V])^2$$

$$v_{GS}^{\,2} + 6v_{GS} + 5 = 0$$

$v_{GS} = -5$, CUTOFF

OR

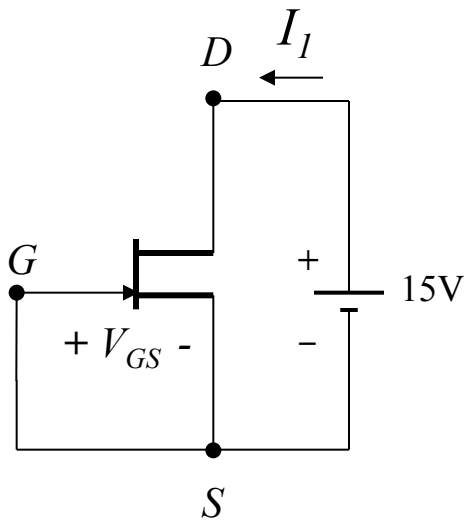
$v_{GS} = -1V$ since $V_{GS} > V_{t0}$

Homework Answers #2

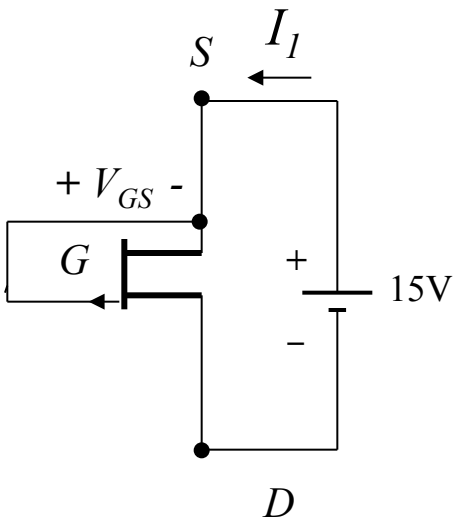
- JFETs
  - Problems: 5.57, V_{to}=*-3 V*
    - Saturation: $v_{DS} \geq v_{GS} - V_{to} \geq -1-(-3)=2V$
    - $v_{DS} \geq -2-(-3)=1V$

Homework Answers #3

- JFETs
  - Problems: 5.65,$|V_{to}|=2\ V$, $I_{DSS}=8mA$



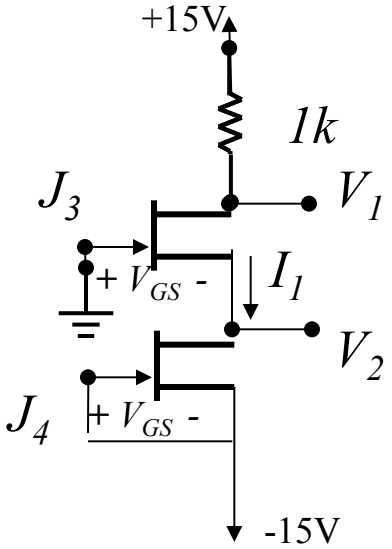
a) $v_{GS}=0$, $I_1=I_{DSS}=8mA$

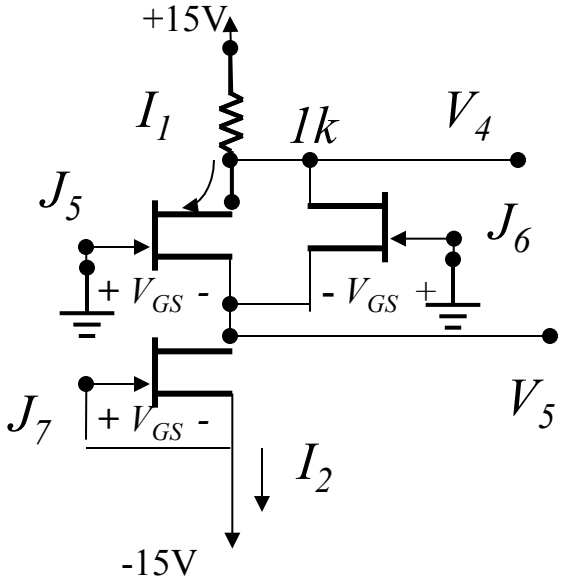


b) $v_{GS}=0$, $I_1=I_{DSS}=8mA$

Homework Answers #4

- JFETs
  - Problems: 5.65, $|V_{to}|=2$ V, $I_{DSS}=8mA$





c)J_4 In Saturation : $v_{GS4}=0$, $I_1=I_{DSS}=8mA$

J_3: Since $I_D=I_{DSS}$, then in saturation and $v_{GS3}=0$, since $V_2=-v_{GS3}=0$ since V_2 is at the source of J_3. $V_{DS4}=15$

Finally, since $I_1=I_{DSS}=8mA$, $V_1=15-1k*8mA=7V$. $V_{DS3}=7$

d) J_7 In Saturation : $v_{GS7}=0$, $I_2=I_{DSS}=8mA$, $V_4=15-8=7V$

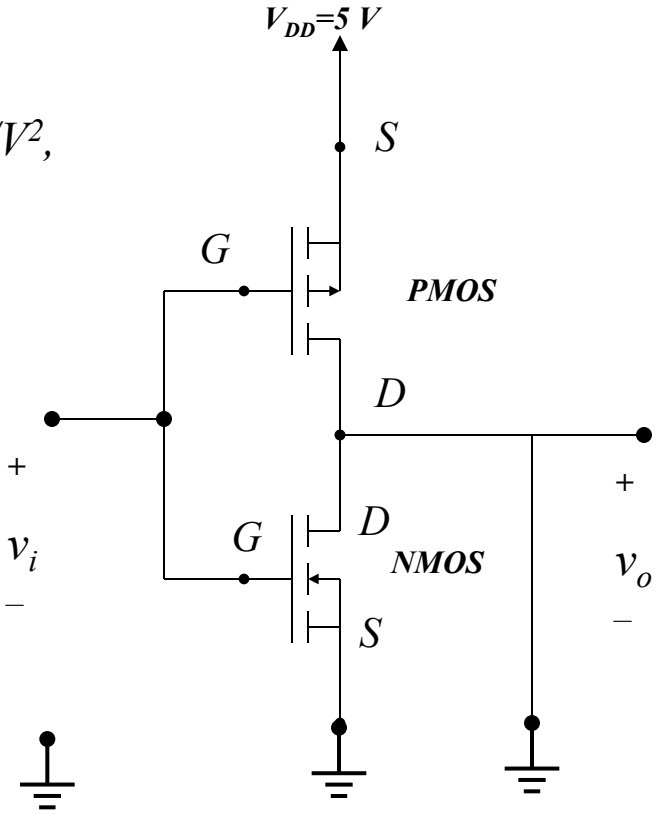
Assume symmetry between J_5 and J_6 and therefore, $I_1=4mA$.

$K=I_{DSS}/V_{to}^2=8x10^{-3}/4=2mA/V^2$; $V_{to}=-2$, $I_1=K(v_{GS5}-V_{to})^2$, we get $v_{GS5}=v_{GS6}=-.5858V$

$V_5=-v_{GS5}=.5858V$

Homework Answers #4

- CMOS Inverter
  - Problems: 6.49 $KP_n=50mA/V^2$, $KP_p=25mA/V^2$, $V_{ton}=1V$, $V_{top}=-1V$, $(W/L)_n=3$, $(W/L)_p=6$
  - Output is grounded; calculate I_{DD} for $V_{DD}=3,5,10$ when $v_i=0$



PMOS now delivers current to ground and $v_{GSP} = -V_{DD}$

$$I_{SHORT} = I_{DP} = K(v_{GS} - V_{top})^2 = K(-V_{DD} - V_{top})^2$$

$$= 75\times10^{-6}(-V_{DD}+1)^2$$

VDD	IDD mA	Power mW
3	0.30	0.9
5	1.20	6
10	6.08	60.75

Homework Answers #5

CMOS Inverter

- Problems: 6.50 If the input is high, how much current does the output sink when $v_o = .5V$, repeat for the input low and the output=4.5 V
  - If the input is high the PMOS is cutoff and the NMOS is in the triode region.

$$i_O = i_D = K[2(v_{GS} - V_{ton})v_{DS} - v_{DS}^2] = 75\times10^{-6}[2(5-1).5-.25] = .281mA$$

  - If the input is low the NMOS is cutoff and the PMOS is in the triode region. Since the transistors are symmetrical, the current is *-0.281 mA*

$$i_o = -i_D = -K[2(v_{GS} - V_{top})v_{DS} - v_{DS}^2] = -75\times10^{-6}[2(-5+1)(-.5)-(-0.5)^2] = -.281mA$$

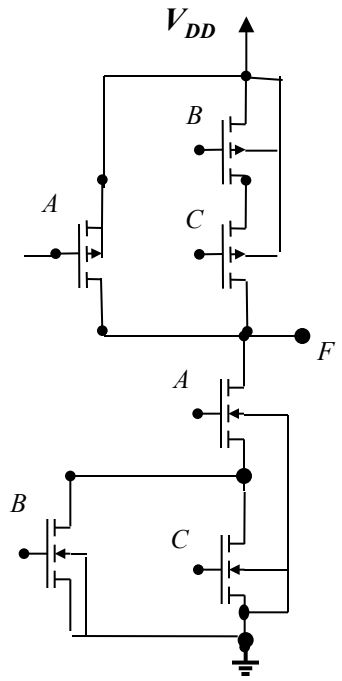
Homework Answers #7

- CMOS Gates
  - Problems: 6.69

$$F = \overline{A(B+C)} = \overline{A} + \overline{(B+C)} = \overline{A} + \overline{B}\,\overline{C}$$

$$note: N_{side} = NA(NB+NC)$$

$$P_{side} = PA + (PB)(PC)$$



Homework Answers #8

– Problems: 6.70

$$F = A \otimes B = \overline{A}B + A\overline{B}$$

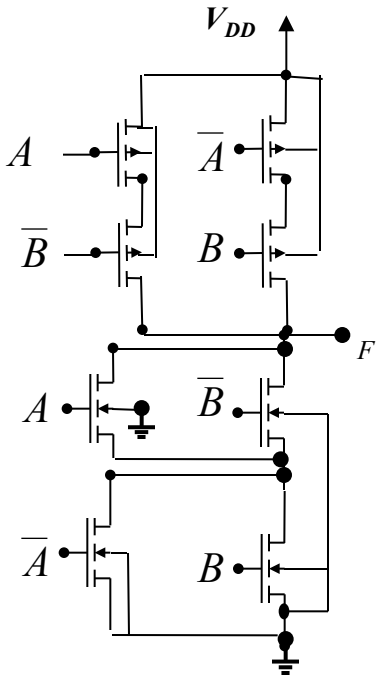
$$\overline{F} = (\overline{\overline{NA}})(NB) + (NA)(\overline{\overline{NB}}) = [(\overline{\overline{NA}})(NB)][(\overline{NA})(\overline{\overline{NB}})]$$

$$= (\overline{\overline{NA}} + \overline{NB})(\overline{NA} + \overline{\overline{NB}})$$

$$= (NA + \overline{NB})(\overline{NA} + NB)$$

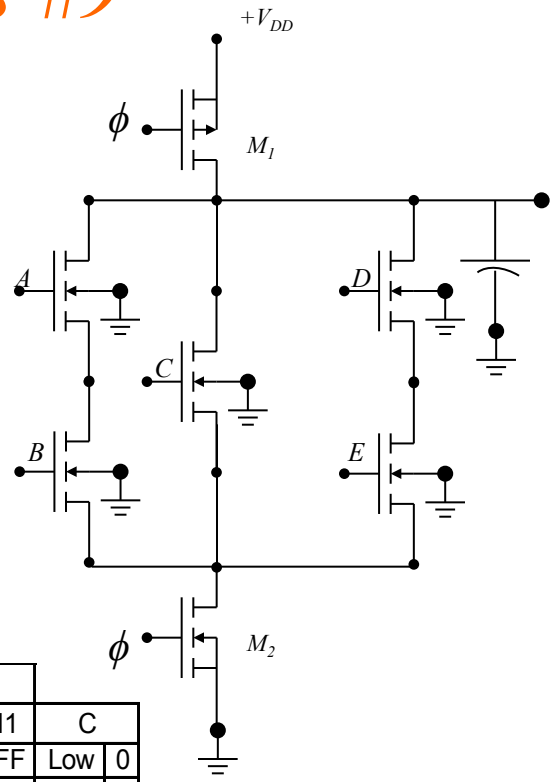
$$Nside = (NA + \overline{NB})(\overline{NA} + NB)$$

$$Pside = (PA)(\overline{PB}) + (\overline{PA})(PB)$$



Homework Answers #9

– Problems: 6.71



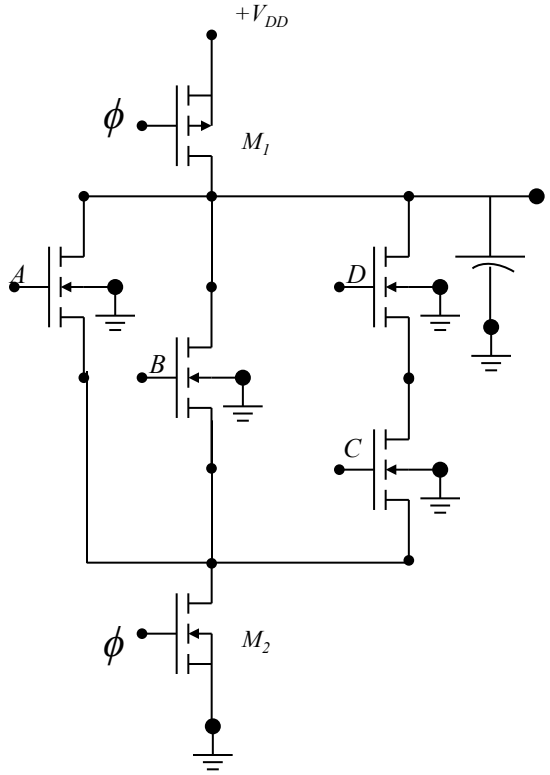
								A	B	C	D	E	P	N		
ϕ	A	B	C	D	E	M2	M1	NA	NB	NC	NC	NE	(NA*NB+NC+ND*NE)M2	M1	C	
1	0	0	1	0	0	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	Low	0
0	0	0	1	0	0	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	High	1

Steady State current is zero since when the PMOS section is off (and the NMOS section in ON) capacitor discharged through the NMOS section and no current is flowing or when the PMOS section is ON (and the NMOS section is OFF) it connected to the capacitor (open circuit).

Homework Answers #10

– Problems: 6.72

$$F = \overline{A + B + CD}$$



Homework Answers #11

– Problems: 6.73

$$F = \overline{(AB + CD)E}$$